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VERTICAL CHANNEL METAL-OXIDE-SILICON FIELD EFFECT TRANSISTOR.(U)
NOV 75 T M HENG, R A WICKSTROM, J G OAKES N00014-74-C-0014
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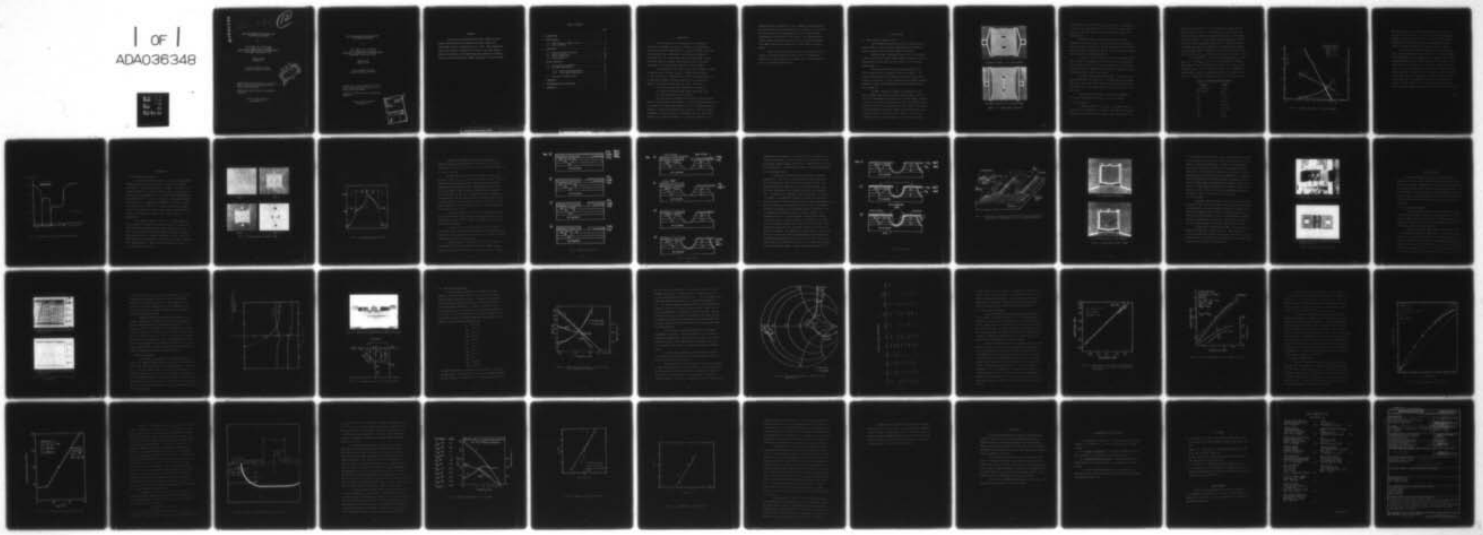

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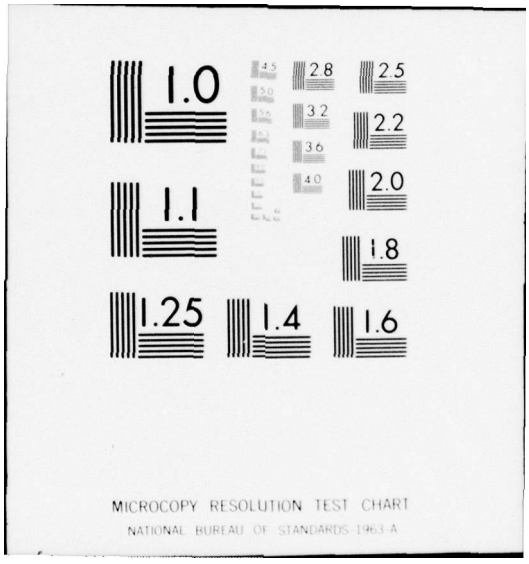
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VERTICAL CHANNEL METAL-OXIDE-SILICON FIELD EFFECT TRANSISTOR

by

T.M.S. Heng, R. A. Wickstrom,
J. G. Oakes, and D. A. Tremere
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Pittsburgh, Pennsylvania 15235

ANNUAL REPORT
1 November 1975

Contract N00014-74-C-0012
Contract Authority NR 251-013

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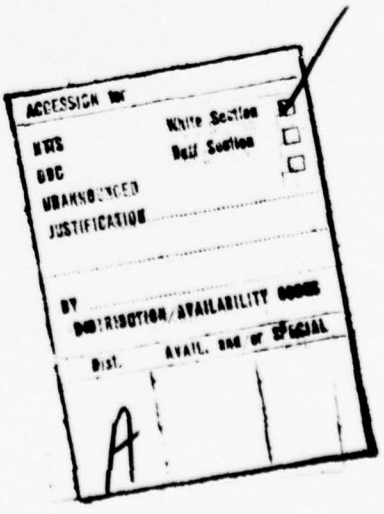

ABSTRACT

Silicon vertical-channel MOS-transistors (VMOST) have been designed and fabricated which exhibited high power capabilities (approaching 5 watts) at frequencies up to 1.5 GHz. Some problems with excess input parasitic capacitance still exist to limit the frequency response of the device, even though significant reductions of parasitic source and gate resistances and feedback capacitance have been achieved.

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1. INTRODUCTION

The main objective of the program was to investigate the feasibility of extending the frequency potential of the Westinghouse silicon vertical channel MOS-field effect transistor (VMOST) to the 2 to 4 GHz frequency band. Additionally, the device must be capable of delivering up to 5 W of output power with an associated gain of 8 dB, have linear amplitude and phase characteristics, and a noise figure comparable to the silicon bipolar transistor at this frequency.

At the beginning of this phase of the contract (N00014-74-C-0012), the maximum cutoff frequency (f_{max}) of the VMOST device was nearly 4.5 GHz, and the Class A output power at 0.5 GHz was approximately 2.5 W. To improve the frequency and power capabilities of the transistor, a number of fabrication problems had to be solved. These were:

(1) Excess gate and source metallization resistances

(2) Excess gate-drain and gate-source capacitances, and

(3) High current and rf power densities.

The first and last problems were effectively solved during the course of the problem by the development of a novel metallization scheme and an extension of the VMOST gate periphery to 1.72 cm. Although significant reductions of gate-drain and gate-source capacitances were made through a tightening of design dimensions, the improvements were not sufficient to influence the frequency performance of the transistor appreciably. The

remaining problem, unfortunately, is more fundamental than had originally been envisaged and may be associated with the low angle ($\sim$15° with respect to surface plane) of gate evaporation used in all the VMOST designs investigated for the most part of the contract. The program, however, yielded valuable information from which several important modifications to the VMOST geometry have been made and are being studied in present devices.

While not all the objectives have been successfully met in this program, it is worth pointing out, however, that the frequency power product that has been achieved by the VMOST device is still state-of-the-art for a silicon MOS transistor today.

2. DEVICE DESIGN

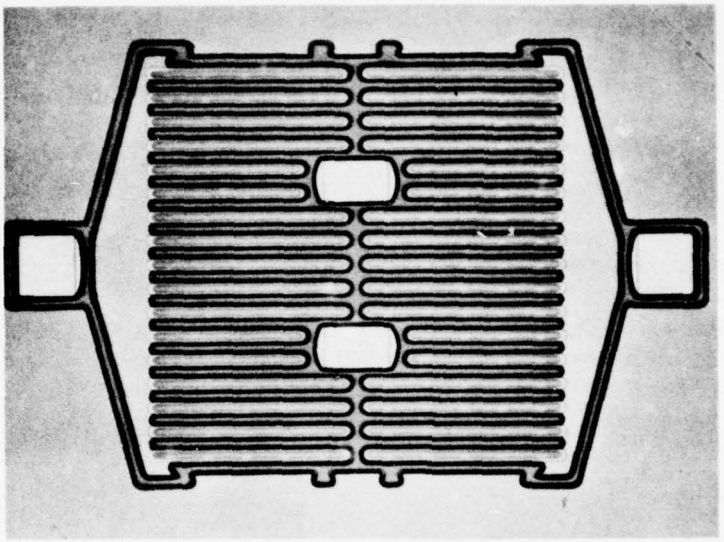
2.1 VMOST Geometries (Mark IV and V)

Two new VMOST geometries (Mark IV and V) evolved from the present study as a result of further understanding of the origins of parasitic capacitive and resistive elements in the device.

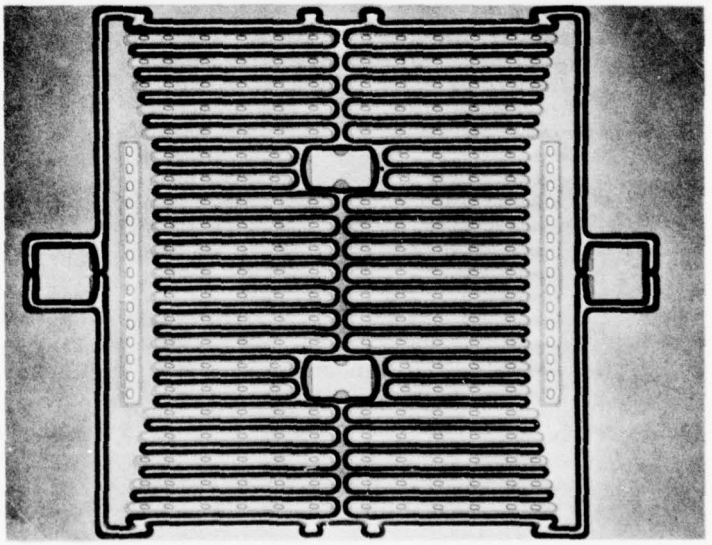
The Mark IV and V transistors, shown in Fig. 1, are similar in many respects to the previous VMOST geometries reported in the last annual report, November 1974, with the exception of the following design changes:

The new devices have an increased gate periphery, from 0.62 cm (Mark III) to 1.3 cm (Mark IV) and 1.72 cm (Mark V). The purpose of this increase is to reduce the operating dc and rf power densities of the device to levels compatible with the maximum operating temperature (120°C) for CW operation and to allow larger rf powers from a single cell.

The Mark V design has a number of improvements over the Mark IV geometry other than the increased gate periphery. While both devices are surrounded by isolation notches, plating bridges consisting of narrow (3 μm) strips of SiO_2 under which the silicon has been etched completely away, have been included in the latest design. The function of these bridges will become more evident with the description of the fabrication process in the next section. Basically, they serve to establish continuity between the gate bus, source contacts, and the



(a) Mark IV Geometry, 1.3 cm Gate Periphery



(b) Mark V Geometry, 1.72 cm Gate Periphery

Figure 1 — S-band VMOST geometries.

outer periphery of the device after metal evaporation. This continuity is used to ensure uniform plating of all the gate and source contacts on the wafer at one time, with the outer periphery metal acting as the plating cathode.

Continuity notches in the gate mesa pad have also been introduced in the Mark V design. These notches ensure uniform metallization of the gate metal up the side and over the top of the gate mesa pad, thus providing reproducible, reliable, and low resistance continuity between the gate bus and gate bonding pad.

As shown in Fig. 1b, a portion of the source bus region in the Mark V geometry is opened down to the n^+ layer to allow low resistance ohmic contact to this area. As in previous geometries, in each active transistor finger p^+ islands are also introduced to ground the p channel to the source metal locally in this region.

The Mark V also has another new feature. The source bus (or source bonding pad) of the device has an internal taper and a straight outer edge. This design feature results in the parasitic gate being deposited directly on the trough instead of along the outer side of the source mesa.

The active area of the Mark V geometry is approximately 0.72 mm by 0.60 mm and the chip die size is 1 mm by 0.89 mm.

2.2 Device Modeling

A computer simulation of an ideal 1.23 cm VMOST design was carried out at the beginning of the program to determine the frequency capabilities of the device in the grounded source configuration. The

results are plotted in Fig. 2. The transistor data used in the simulation are given in Table I. The dotted curves in Fig. 2 are the intrinsic transistor characteristics (negligible parasitic source, drain, and gate resistances). Over the whole frequency passband up to 10 GHz, the device is only conditionally stable ($K < 1$). Under this condition, the highest gain that can be achieved is the maximum stable gain (MSG). For the frequency range of interest (2 to 4 GHz), this gain is at least 10 dB. The intrinsic f_{max} ($U = 0$ dB) of the device is in excess of 20 GHz.

In the presence of finite contact resistances ($R_{source} = 0.25\ \Omega$, $R_{gate} = 0.5\ \Omega$, and $R_{drain} = 0.25\ \Omega$) a severe degradation of frequency-gain response is seen. The device as expected is more stable, and for frequencies above 7 GHz, K is greater than unity, or the transistor is unconditionally stable. The unilateral gain fall off, however, is in excess of -12 dB per octave and the device cuts off at nearly 9.5 GHz.

Table I - S-band Power VMOST Parameters

Elements	Values
Gate periphery	12,320 μm
Gate length	0.8 μm
C_g	3.7 pf
R_g	1.4 ohms
C_{dg}	0.73 pf
g_m	0.28 mhos
g_d	10 millimhos
C_{ds}	5.2 pf
R_{on}	3 ohms

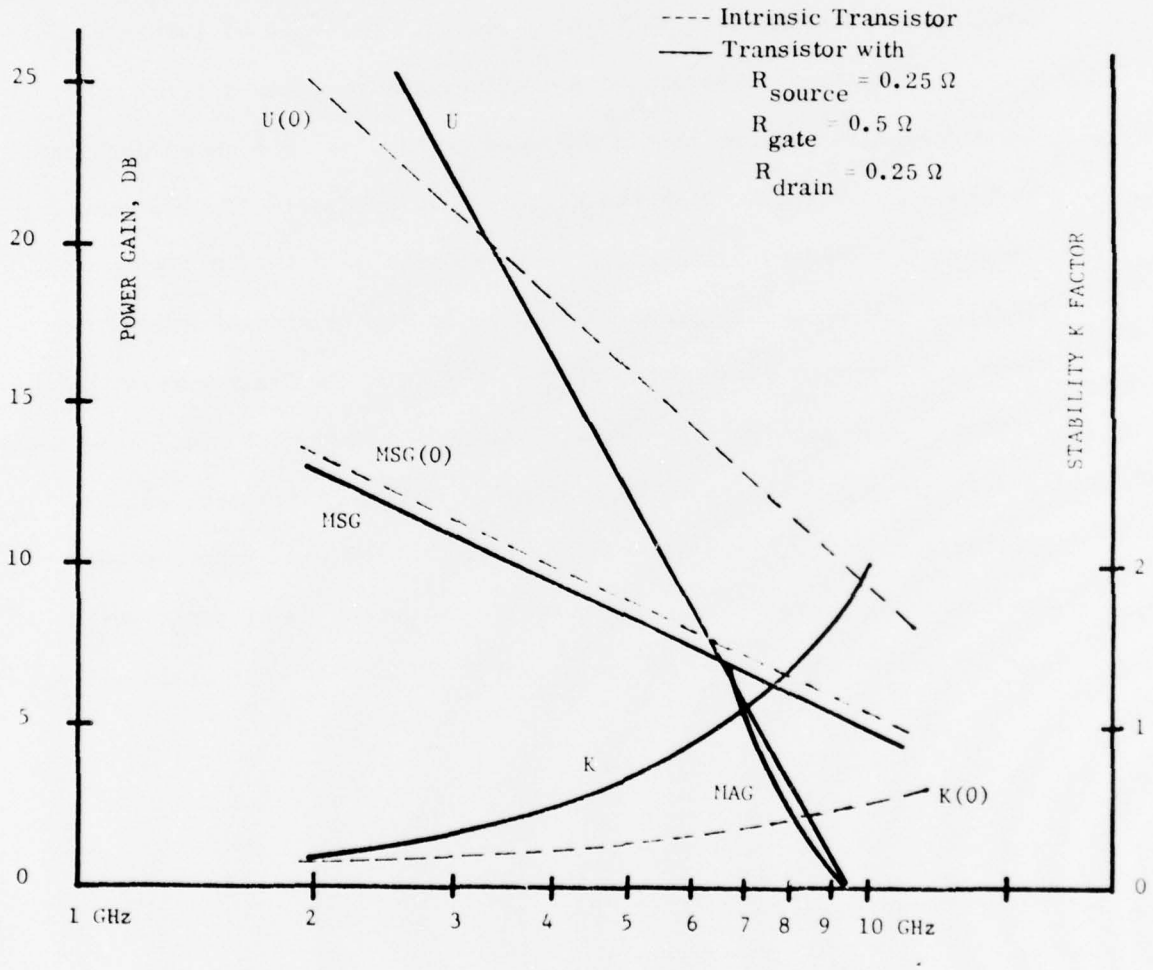


Fig. 2 — Computer Simulation of S-band Power VMOST

The maximum stable gain, on the other hand, is barely perturbed by the presence of these parasitics. In general, the stability and maximum frequency are fairly sensitive to device parasitics, in particular R_S. Nevertheless, the studies do show that the proposed VMOST design is capable of operating well above the frequency passband of interest.

The transistor parameters calculated for this initial model had a concentration profile as sketched in Fig. 3. The short p-channel (0.8 μm) was chosen to give the device an f_T of nearly 13 GHz, assuming a scattering limited surface electron velocity of 6.5×10^6 cm/s. The length of the n^- drift region was 1.5 μm to give a transit delay time of only 23 ps or a phase delay of the short circuit drain current with respect to the gate voltage of 16.6° at a frequency of 4 GHz. This delay is sufficiently small as to be negligible except at frequencies much greater than 4 GHz. The breakdown voltage of the $p\text{-}n^-$ junction was assumed to be approximately 30 volts from previous VMOST data, which gives a p depletion width of approximately 0.3 μm at this drain voltage.[1]

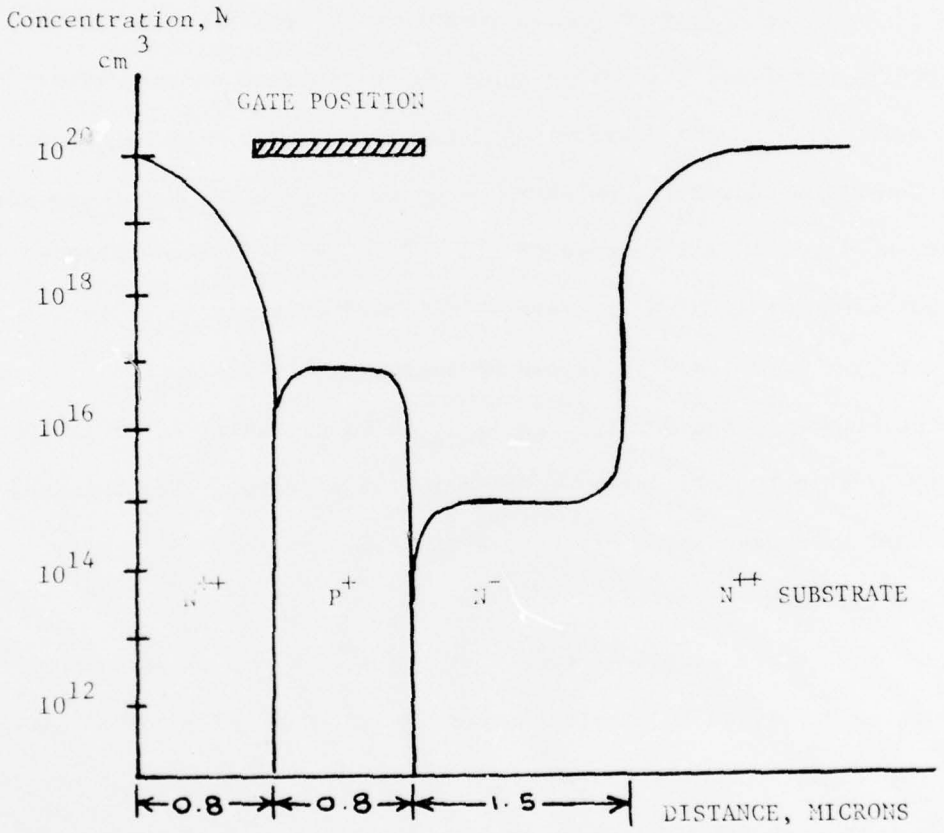


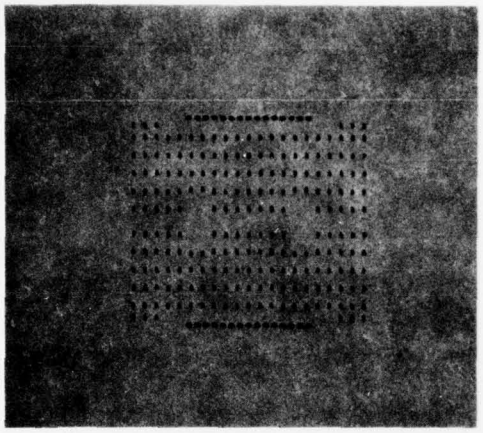
Fig. 3 — Concentration Profile for S-band Power VMOST

3. FABRICATION

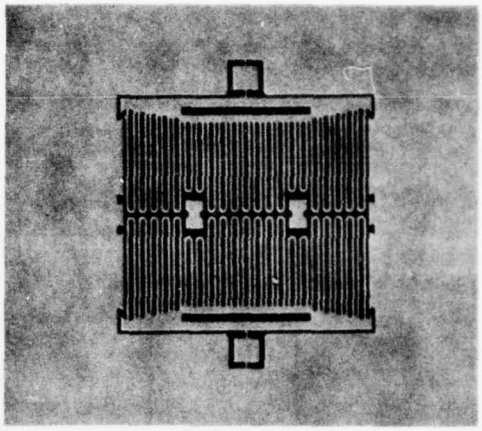
3.1 Silicon Material Processing

The epitaxial growth technique for realizing the S-band VMOST impurity profile, Fig. 3, is essentially the same as that reported previously.[1] The starting material is a <0.008 Ω-cm As-doped n^+ <111> orientation substrate, on which is grown by chemical vapor deposition the n^- layer to a thickness of 1.5 - 2 μm and a doping concentration of approximately 10^{15} cm^{-3}. This is followed by a second epitaxial growth of p-type layer to a thickness of approximately 1.4 μm and a concentration between 3 and 5 x 10^{16} cm^{-3}. A third epitaxial layer is grown on top of this to form the p^+ contact to the p region. The thickness and impurity concentration of this layer is 0.5 μm and $>10^{18}$ cm^{-3}, respectively.

After epitaxial growth of the n^- - p - p^+ layers, 5000 Å of SiO_2 is deposited by chemical vapor deposition (CVD) on the wafer and photolithographically delineated into islands using Mask 1, Fig. 4. The wafer is next subjected to a shallow phosphorus diffusion to a depth of approximately 0.8 μm at a deposition temperature of 1150°C. This diffusion forms the n^+ source contact, while leaving p^+ islands for grounding the p channel substrate. Figure 5 shows the spreading resistance profile of a typical wafer after this step.



Mask 1



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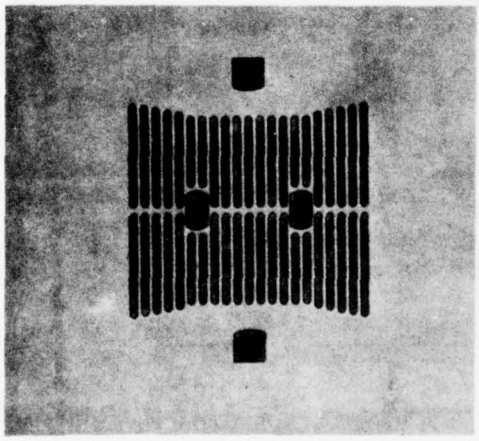

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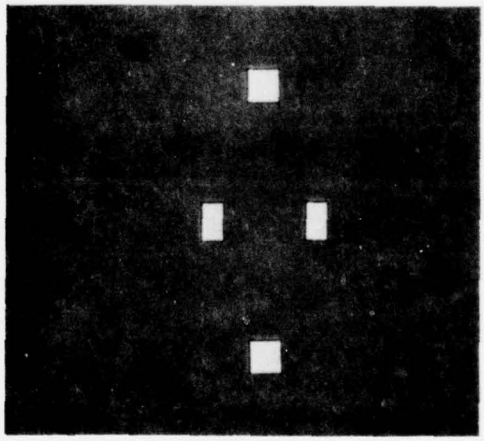


Mask 4

Fig. 4 — Processing Masks for Mark V VMOST

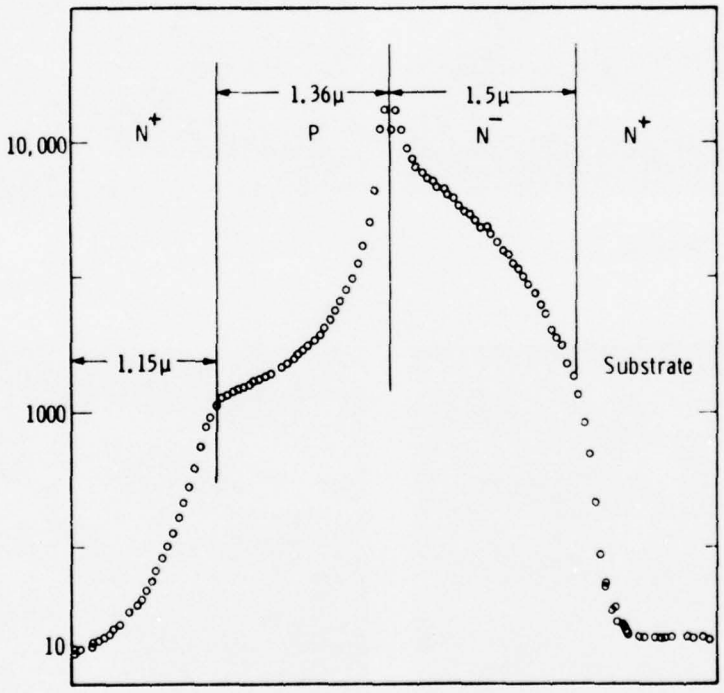


Fig. 5 — Spreading Resistance Profile

Following the phosphorus diffusion, the SiO_2 islands are removed by chemical etching and another CVD SiO_2 layer, 0.7 μm thick, is deposited on the wafer. The latter is now ready for device processing.

3.2 *Device Processing*

The VMOST processing steps are illustrated in Fig. 6. The first nine steps, Steps A to I, are exactly the same as before [1] and are described here for completeness sake. The first step in the device fabrication is the delineation of the VMOST geometry, Mask #2, Fig. 4, after which 1000Å of Si_3N_4, followed by 1600Å of SiO_2, are deposited over the SiO_2 pattern, Fig. 6A. A second SiO_2 pattern is defined photolithographically, Mask #3, and etched down to the Si_3N_4 layer, Fig. 6B, to form an etch mask for the Si_3N_4. The wafer is now etched in a commercial phosphoric acid solution "Transetch-N" to remove the Si_3N_4 down to the silicon level, Fig. 6C.

A fourth mask, Mask #4, is used to selectively etch away the SiO_2 layer covering the Si_3N_4, Fig. 6D, in the gate mesa pads. The exposed silicon is then etched to a depth of approximately 5 μm, Fig. 6E, down to the n^+ substrate.

In Step Fig. 6F, the Si_3N_4 on the gate mesas are removed, followed by a quick etch in buffered HF to remove the remaining SiO_2 mask layer on the source fingers, Fig. 6G. The wafer is now ready for thermal oxidation to form the thin MOS gate oxide.

Thermal oxidation is carried out at 850°C in wet oxygen for a total period of 55 min, during which between 950 to 1000Å of SiO_2 is grown over the exposed silicon surface, as shown in Fig. 6H. The Si_3N_4

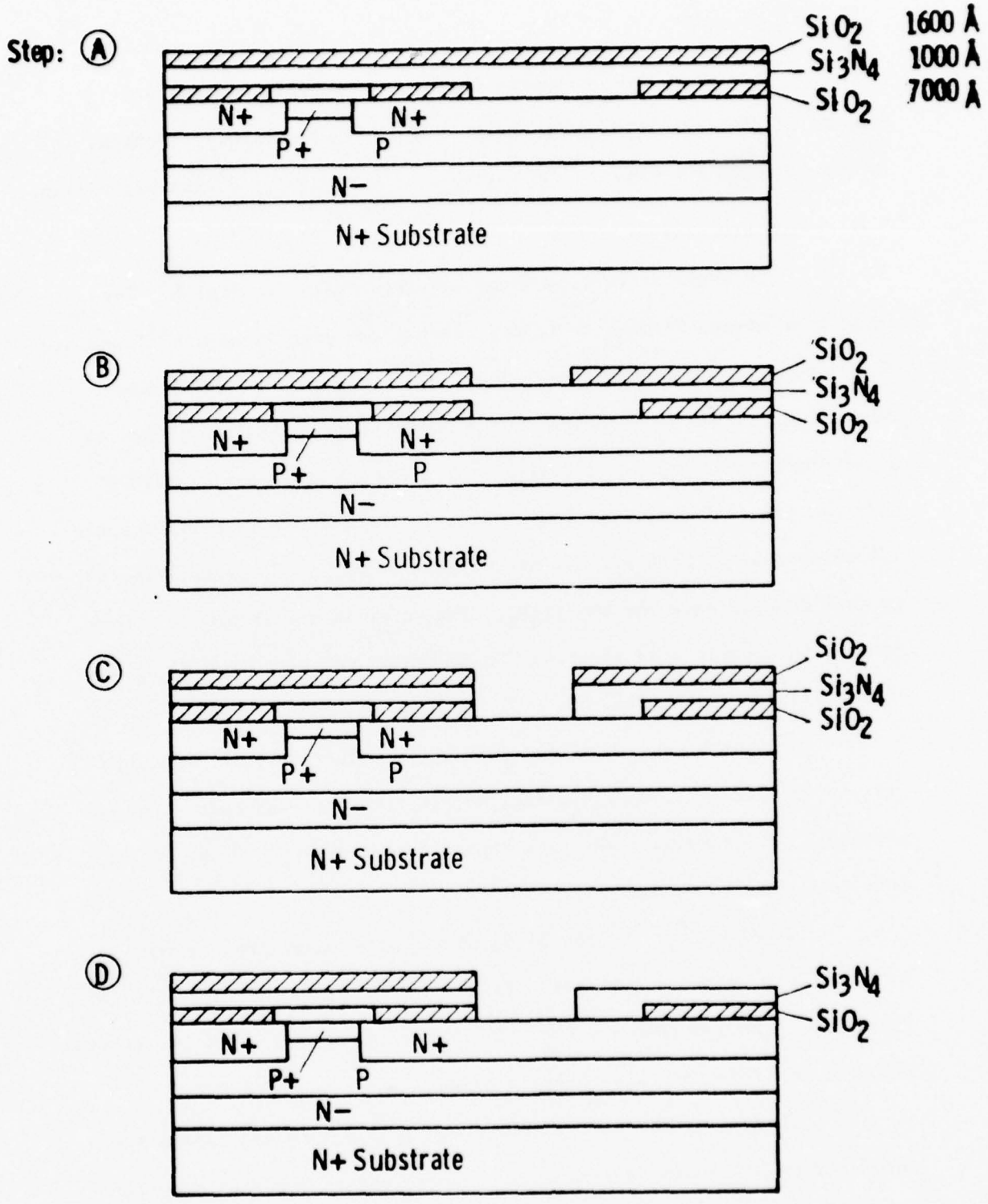


Fig. 6 - VMOST Processing Steps

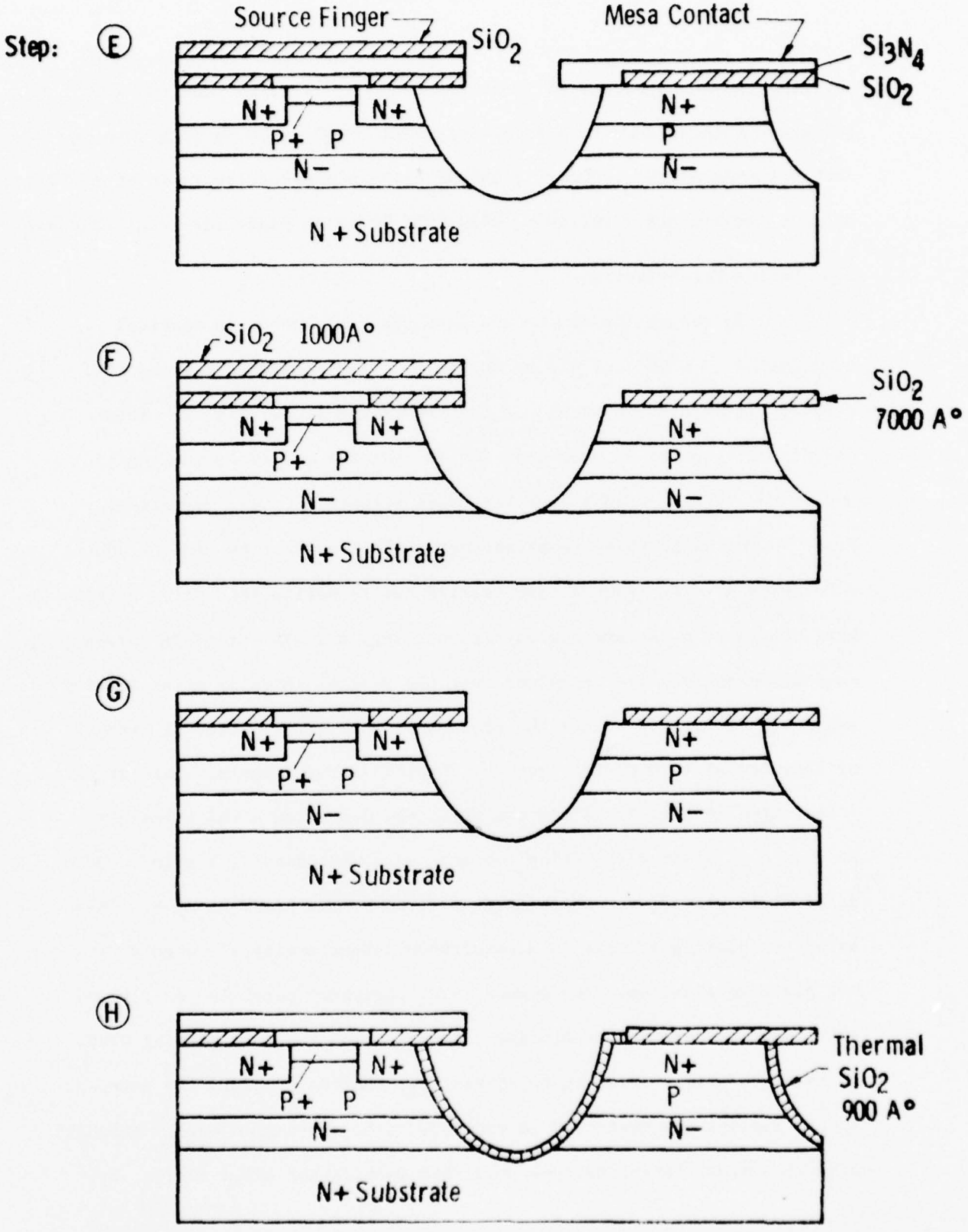


Fig. 6 (Continued)

covering the source openings is next etched off, Fig. 6I, and the wafer substrate thinned down to a final thickness of 25 to 30 μm in a rotating etch solution of HNO_3, $HC_2H_3O_2$, and HF using a composition ratio of 25:10:1 at room temperature. Following this, the wafer is ready for metallization.

3.3 Device Metallization

To reduce the source and gate bus resistances, a vertical evaporation ($\theta = 90°$) of Aℓ, up to 0.6 μm thick, is first carried out. This is illustrated in step J of the processing steps, Fig. 6. This additional evaporation step deposits Aℓ over the entire source region and in the trough regions over the drain between the SiO_2 overhangs, Fig. 7. Following this, complementary angle evaporations of Cr (1200 Å) - Pd (6000 Å) - Au (6000 Å) are carried out to define the active gates, gate bus, gate pads, and source regions, Fig. 6K. The Cr-Pd-Au metals in the last three regions are deposited over the initial thick Aℓ metallization and act as a metal mask for the subsequent removal, by chemical etching, of unwanted Aℓ from regions between the transistor fingers. This is illustrated in Fig. 7. Since the angularly deposited metal thickness is only $2\ t_g \times \text{Sin}\ \theta$ (t_g being the gate metal thickness), a thin (2000 Å) Au layer is plated over those areas covered by the Cr-Pd-Au mask. This selective plating process is accomplished automatically since gold does not plate to aluminum. The common outer periphery metal is readily available so it is used as the plating cathode during the gold plating step. To maintain uniform plating thickness over the whole wafer, the gate and source regions are connected in each device to the common outer periphery area by narrow plating bridges described earlier and shown in Fig. 8a.

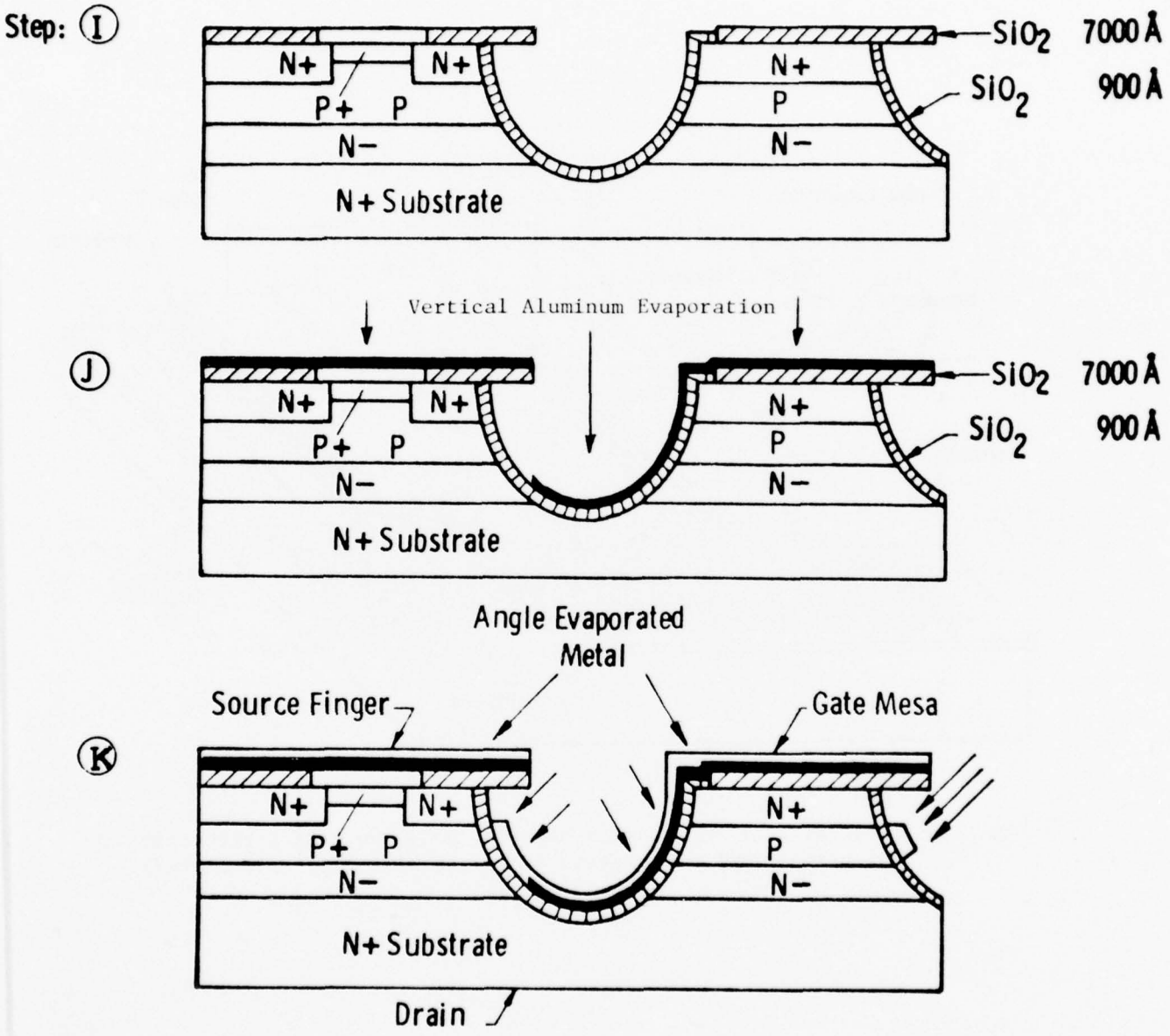


Fig. 6 (Continued)

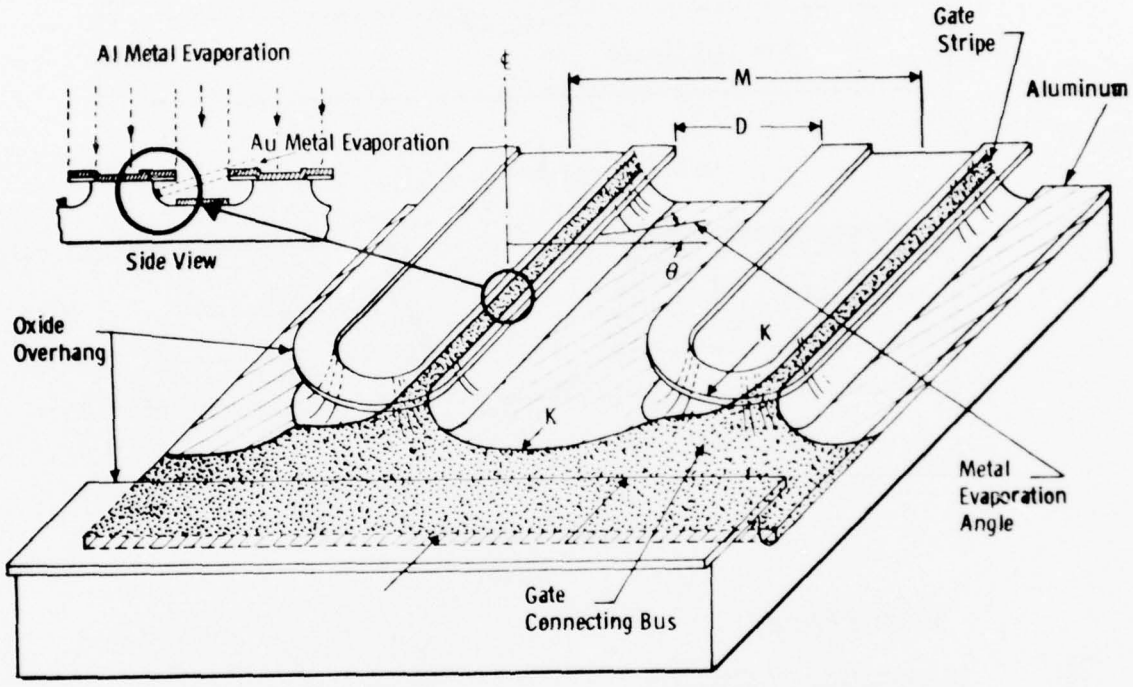
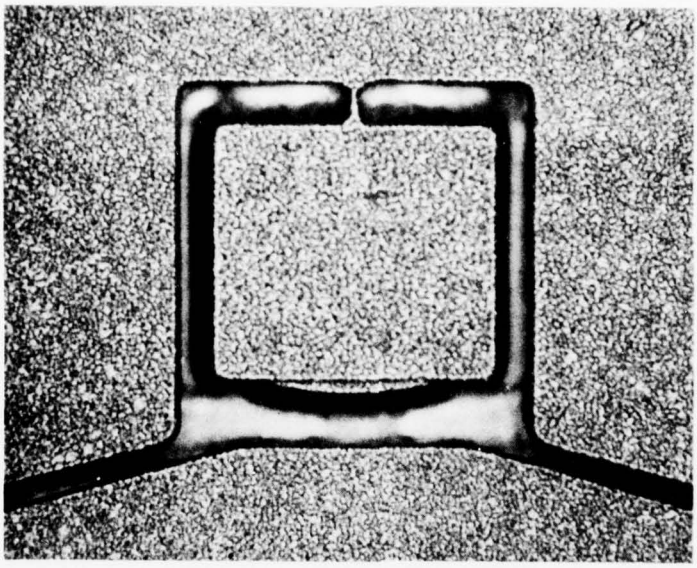
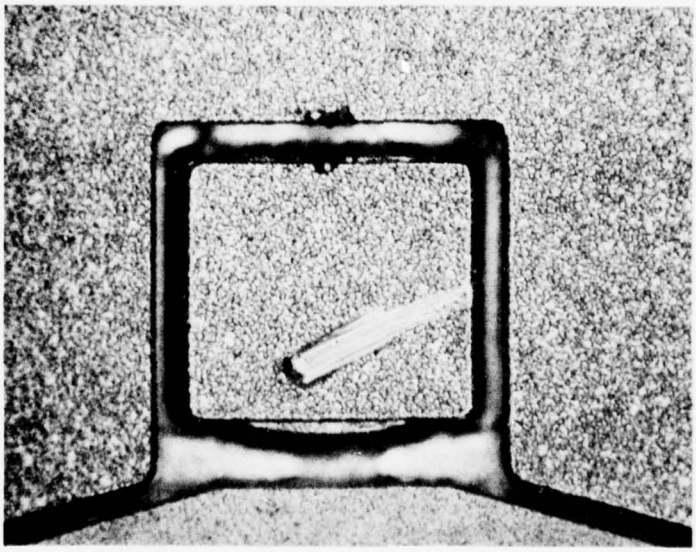


Fig. 7 — Ghost view of fabrication of VMOST gate and gate interconnection bus using slant evaporation (only one side shown evaporated).



(a) Bridge after Au plating



(b) Bridge opened by current pulsing

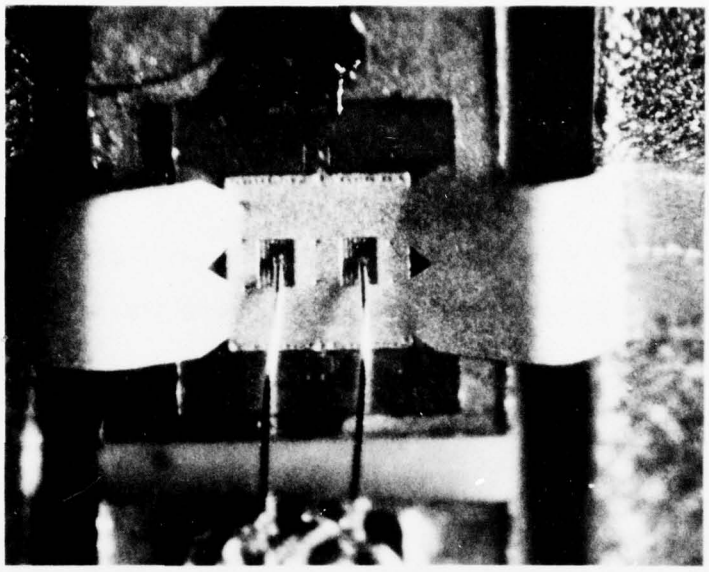
Fig. 8 — Plating Bridge in Mark V VMOST

In the finished devices, therefore, the gate bus and source resistances are governed by the thick vertical aluminum evaporation, and not by the angularly deposited Cr-Pd-Au metals. Because of this, the measured effective gate and source resistances are now typically 0.2Ω and 0.1Ω respectively. This represents a reduction of greater than one order of magnitude in both resistances over previous VMOST devices. During the final fabrication steps the unwanted aluminum is chemically etched away and the plating bridges are opened during dc testing by pulsing a high current (∿ 1 amp) through the bridge metal to evaporate the thin metallization, Fig. 8b. This step is trivial and completely reproducible, and appears to have no effect on device characteristics.

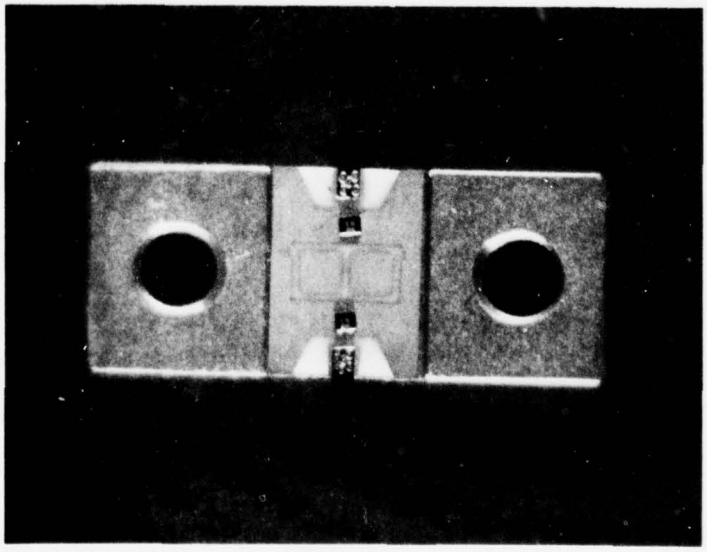
3.4 Device Bonding

Diced VMOST chips are bonded to BeO chip carriers mounted on Au-plated Cu studs. The chip is mounted directly onto the drain terminal and connections to the source terminals are made by a Au-plated 0.001 in. thick preform ribbon as shown in Fig. 9a. This allows the source inductance to be minimized (below 0.05 nh) for high frequency performance and helps in removing heat from the die. Connections to the gate pads are made through openings in the preform with 0.0015 in. Au wires.

Chip carriers for paralleling two VMOST cells have also been designed and fabricated, as shown in Fig. 9b. These carriers have provisions for MOS chip capacitors which could be used in device matching. Work on multiple cell internally matched VMOST devices is currently going on and should be completed in the near future.



(a) Single device package with Au-plated preform source ribbon



(b) BeO chip carrier for two VMOST chips with MOS matching capacitors

Fig. 9 — Chip Carrier VMOST Packages

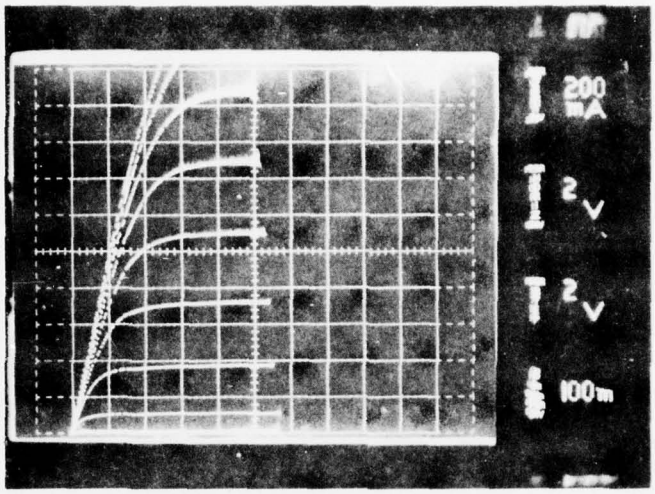
4. DEVICE EVALUATION

The fabricated VMOST devices were carefully tested at low frequencies for their current-voltage and capacitance-voltage characteristics and at microwave frequencies for their small signal S-parameters. Devices from good wafers were tested for their power capabilities. Tests were also made on one device series to measure intermodulation product and noise figure. Small-signal models of the VMOST devices were derived from the measured data and used to pinpoint the areas needing further improvement.

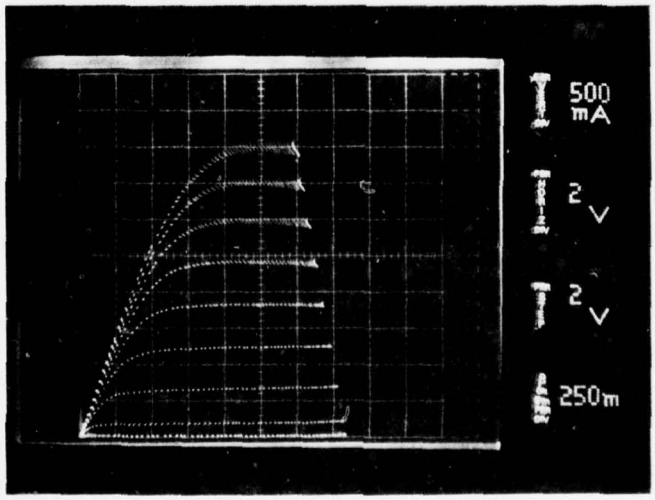
4.1 Low Frequency Measurements

A Tektronix 576 curve tracer was used to observe the output characteristics, breakdown voltages and leakage currents of each device. The gate leakage current was monitored using a Keithley 413A micromicroammeter and the input, output and feedback capacitances were measured at 1 MHz using a Boonton 72AD capacitance meter.

Figure 10 shows the dc drain current-voltage characteristics of a typical Mark IV and a Mark V VMOST device. The saturated current is nearly 2A at a gate voltage of 16V for the first design, and 3A at the same gate voltage for the second design. The maximum transconductances (g_m) are 0.2 mho and 0.3 mho, respectively. These give a transconductance per unit gate periphery (g_m/W) of 15.4 and 17.4 micromhos/micron consistent with a channel saturation electron velocity between 5 and 6 x 10^6 cm/s.



(a) Mark IV Transistor, 1.3 cm Gate Periphery (VMOST 28-3)



(b) Mark V Transistor, 1.75 cm Gate Periphery (VMOST 29-3)

Fig. 10 — I-V Characteristics of VMOST Devices with 900Å SiO_2

If the probe resistance of 1.1 ohm is subtracted in each case, the minimum turn-on resistances of the devices are 1.3 and 0.6 ohms respectively at the gate voltage of 16V. These are the lowest resistances that have been reported to date from an MOS device, and opens up the possibility of using the VMOST device for high speed microwave switching applications.

Significant progress has been made in the reduction of the feedback capacitance of the VMOST devices. The typical C_{gd} of the 0.63 cm periphery VMOST devices reported previously was 6 pF. The typical C_{gd} for the 1.72 cm Mark V device was measured to be between 3 and 6 pF, in spite of the factor of three increase in the gate periphery. The feedback capacitance per unit gate periphery has thus been decreased by at least this factor. This contributed directly to an increase in the Maximum Stable Gain (MSG) and stability factor (K) of the larger periphery devices. Figure 11 shows the typical measured 1 MHz capacitance-voltage characteristics of a Mark V device.

4.2 Microwave Measurements

The microwave characterization of the VMOST devices was performed using a Hewlett-Packard 11608A test jig for which a special water-cooled copper block was machined to fit the VMOST headers, as shown in Fig. 12. Bias was supplied using the internal bias provisions of the HP8746B S-parameter test set or by a pair of HP11590A bias networks. The small-signal measurements included gain, frequency response and noise figure and allowed an accurate model of the VMOST device to be developed, Fig. 13. The large-signal measurements included intermodulation product (IMP) and power tests.

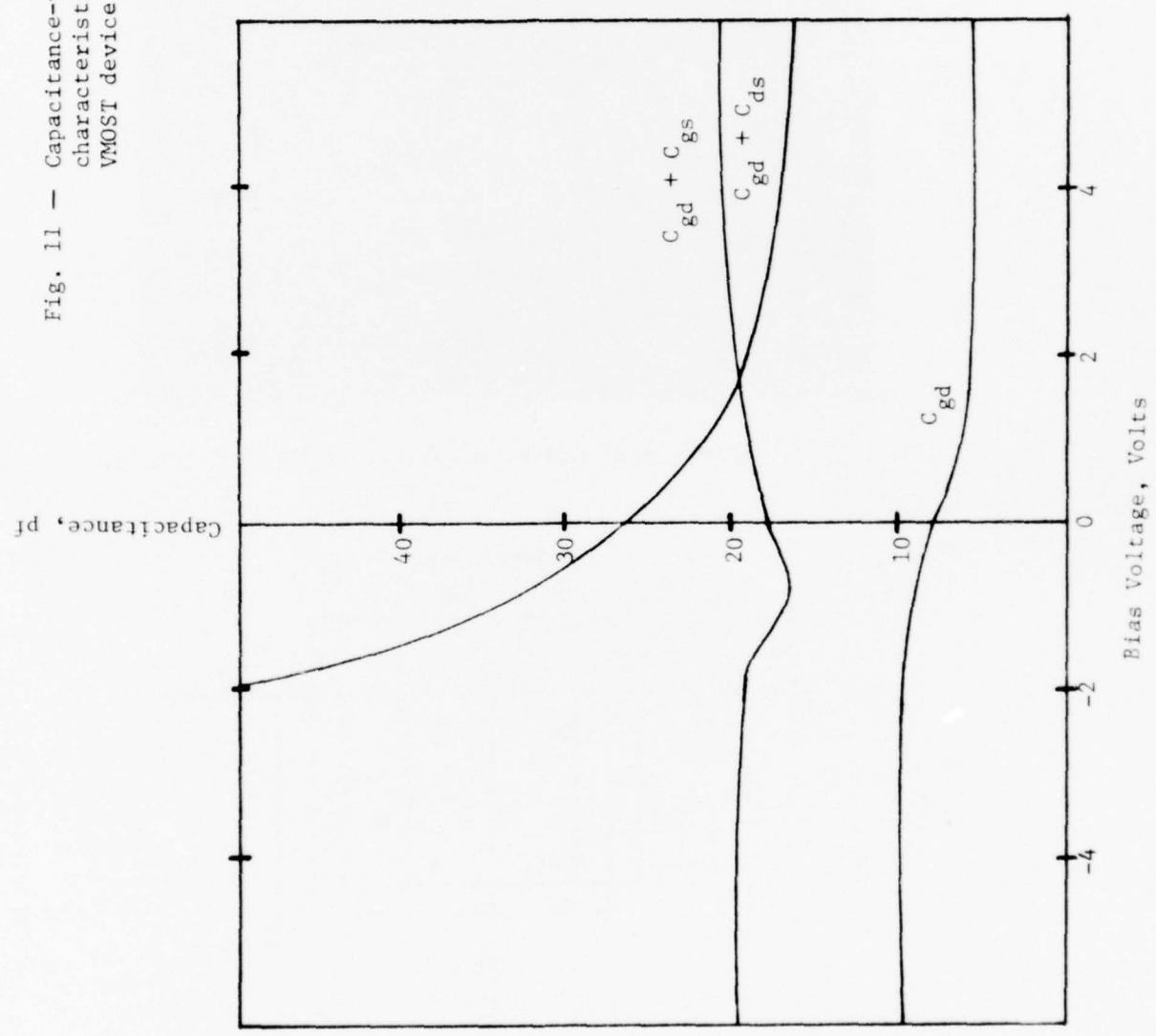


Fig. 11 — Capacitance-voltage characteristics of Mark V VMOST device

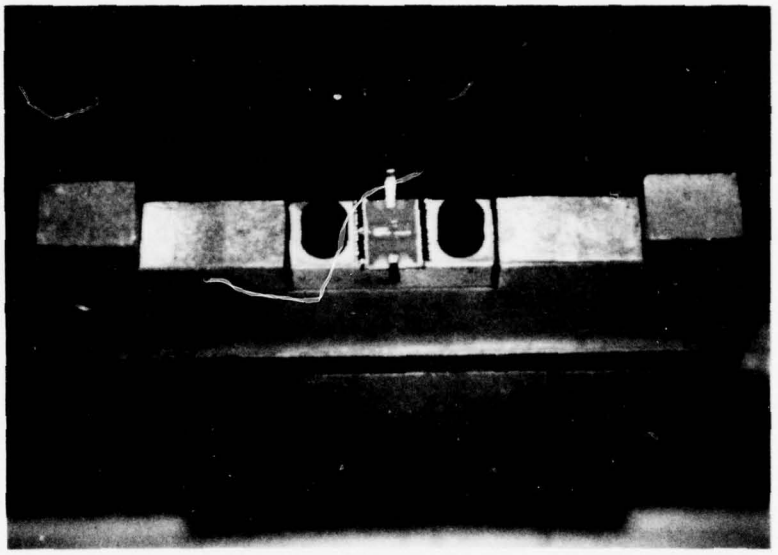


Fig. 12 — Water-cooled Copper Block for VMOST Chip Carrier

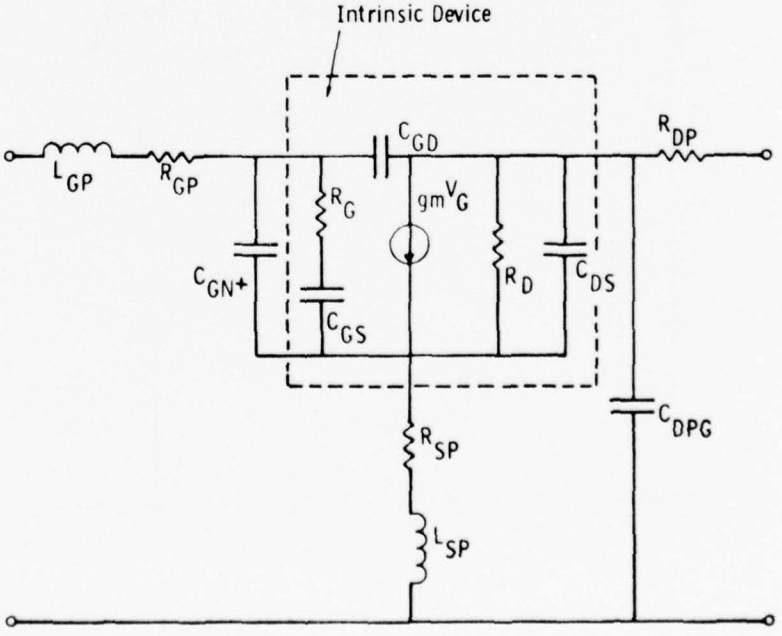


Fig. 13 — Equivalent Circuit Model for VMOST Devices

4.2.1 Small Signal Measurements

The small signal S-parameters of the VMOST devices were measured on an HP 8410 Network Analyzer and an internal Westinghouse computer program converted the results to Y-parameters, Z-parameters, and various gain and stability parameters. The gain and stability of a Mark IV VMOST device (#28-3-19), for example, are shown in Fig. 14. The extrapolated f_{max} of this device was 3.5 GHz and the available gain was 5 dB at 1.5 GHz. The dashed line in the figure represents the predicted behavior based on the small signal model shown in Fig. 13. The parameter values used for the simulation were

g_m = 0.21 mho

C_{gs} = 5.13 pF

C_{ds} = 12.6 pF

C_{gd} = 5.6 pF

C_{gn} = 8.6 pF

R_g = 1.7 Ω

R_d = 40 Ω

R_{gp} = 0.5 Ω

R_{sp} = 0.1 Ω

R_{dp} = 0.1 Ω

L_{gp} = 0.178 nH

L_{sp} = 0.15 nH

The biggest improvement in this device is the reduction of the source and gate parasitic resistances due to the vertical aluminum evaporation discussed previously. Using the values of measured resistances in the

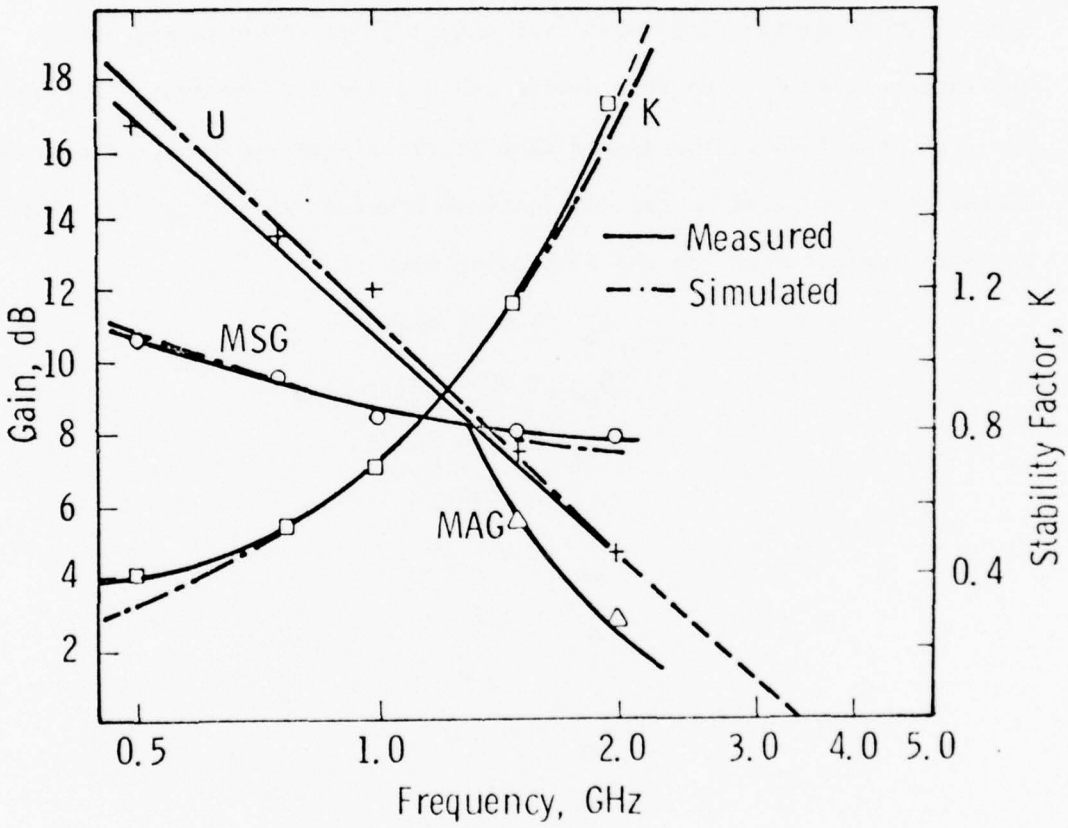


Fig. 14 — Small signal characteristics of Mark IV device 28-3-19 measured and simulated

Mark III device and scaling them to correspond to an equivalent 1.3 cm periphery device leads to a predicted source resistance, R_{sp}, of 1 to 2 Ω, while the VMOST 28-3 device had only 0.1 Ω. The scaled value of R_{gp} without the aluminum evaporation was 2 Ω, while VMOST 28-3 had only 0.5 Ω. The vertical aluminum evaporation has thus reduced the resistive losses by a factor of 10 or more in the source and by a factor of 4 in the gate corresponding to a reduction of gate bus resistance. Besides increasing the gain of the device, the reduction of the source resistance has improved its stability and eliminated the spontaneous oscillations which were observed in some previous VMOST devices when they were tuned for power measurements.

Of more interest to amplifier application are the actual S-parameters of the device. These are shown in Fig. 15 for both the measured and modeled device. Notice that both S_{11} and S_{22} are near the outside of the Smith chart, indicating that the parasitic losses are low. For clarity, the values of S_{12} shown are ten times the measured values.

The small signal performance of the Mark V devices has been equally impressive and the results obtained are summarized in Table II, which will be discussed in Section 4.3.

The noise figure of several 28-3 devices has also been measured at 1 GHz using an AIL Type 75 Precision Automatic Noise Figure Indicator. The devices were dc biased for these tests at relatively low drain currents (<0.5A) to minimize heating. The measured noise figures were typically between 5.5 and 6 dB. Considering that these are large periphery

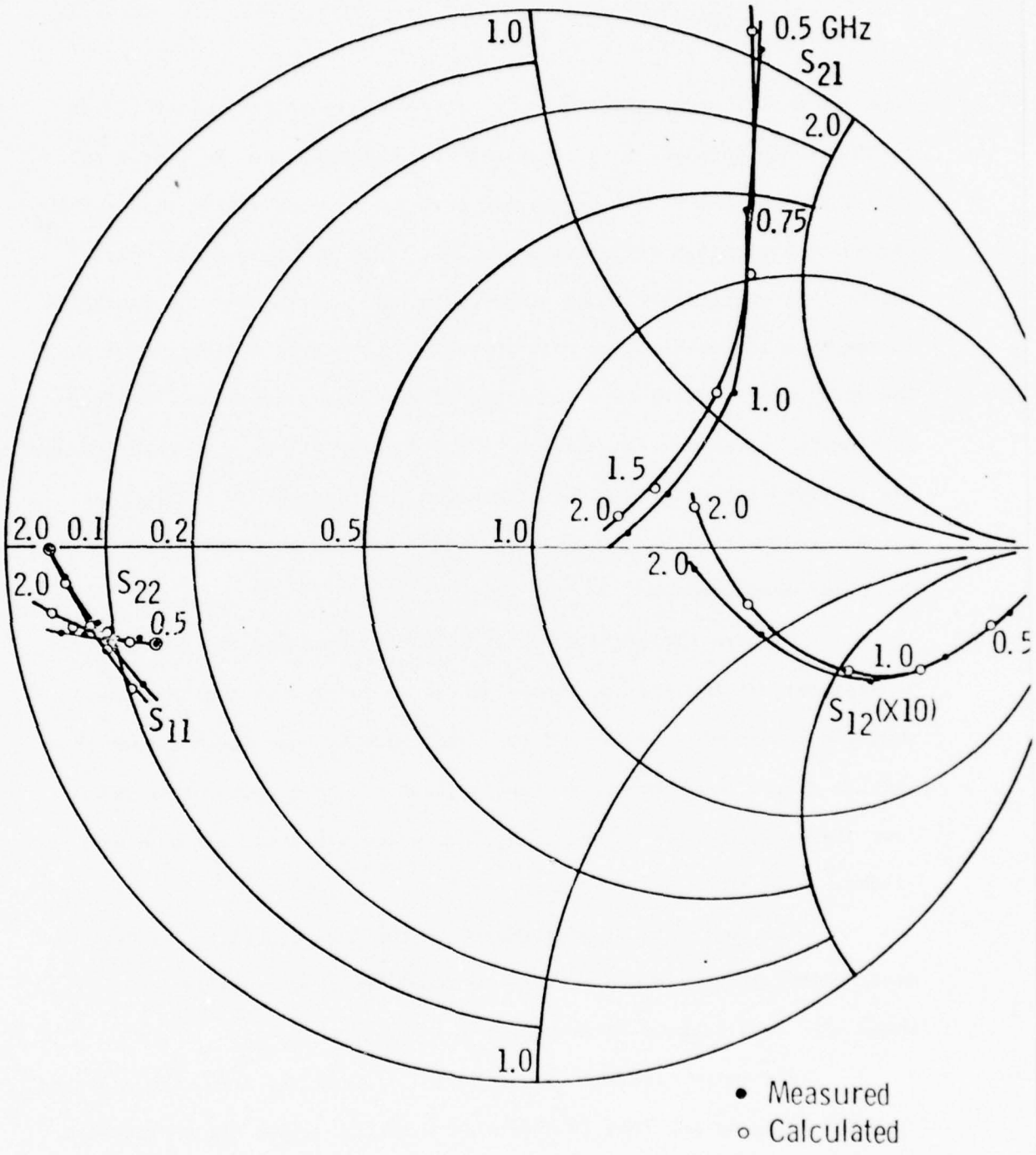


Fig. 15 — Measured and Calculated S Parameters 1.32 cm
VMOST 28-3-19

Table II - Table of VMOST Runs

Run	C_{GS}	C_{DS}	C_{GD}	G_m	W_{n^-}	P Depth	P Width	θ Angle	Slit Width	f_{max}
28-3	15	15	5	180	low N^-	1.9	0.62	78	5.5	1.8
	(20)	(20)	(6.7)	(242)						
31-1	10	10	2.5	130	low N^-	2.42	1.26	78	4	--
31-2	12	13	3	270	low N^-	1.7	0.34	78	4	3
32-3	16	7.2	2	100	--	--	--	78	3.5	--
33-3	15	10	6	260	low N^-	1.67	0.86	78	5	2
34-2	20-21	13-15	5	230	1.13	2	0.88	77.5	4.75	--
34-4	23	9	7.5	230	1.62	2	1.2	78	4.5	--

(1.3 cm) power devices, these values are commendably low and are comparable to the 4 dB noise figure at 1 GHz reported by Sigg et al.[2] for a 700 μm periphery D-MOS transistor. These devices were all tuned for maximum gain at 1 GHz and no attempt was made to optimize the noise figure by varying either the tuning or bias point of the device.

4.2.2 Large Signal Measurements

Devices from three wafers have produced significant power at 1 GHz or higher. The power capability of a 1.3 cm periphery device, #28-3-39, is shown in Fig. 16. Operating Class AB at 1 GHz, this device showed a linear gain of 6.2 dB and an output power of 2.8 W at 1 dB compression (5.2 dB gain). The drain efficiency of this device was 31% at the 2.8 W point and the power-added efficiency was 21%. These results represent a substantial improvement over the 2 W at 0.5 GHz and 6 dB gain which was obtained with the best Mark III device.

The power characteristics of a 1.75 cm Mark V device at 1.56 GHz are shown in Fig. 17. This device was operated Class AB so the gain rises as the input power is increased and peaks at almost 6 dB. At the 1 dB compression point (5 dB gain), the output power is 3 W, the drain efficiency is 48%, and the power-added efficiency is 32%. This device operated a half-octave higher in frequency than the best Mark IV devices and had a 10% higher power-added efficiency. The gain at 2 GHz was approximately 4 dB. The magnitude of the power produced, however, was no higher than that of the 1.3 cm device. This can be explained by a deficiency in the doping profile of the wafer which, while not affecting the frequency response, limited the drain breakdown voltage to less than 20 volts.

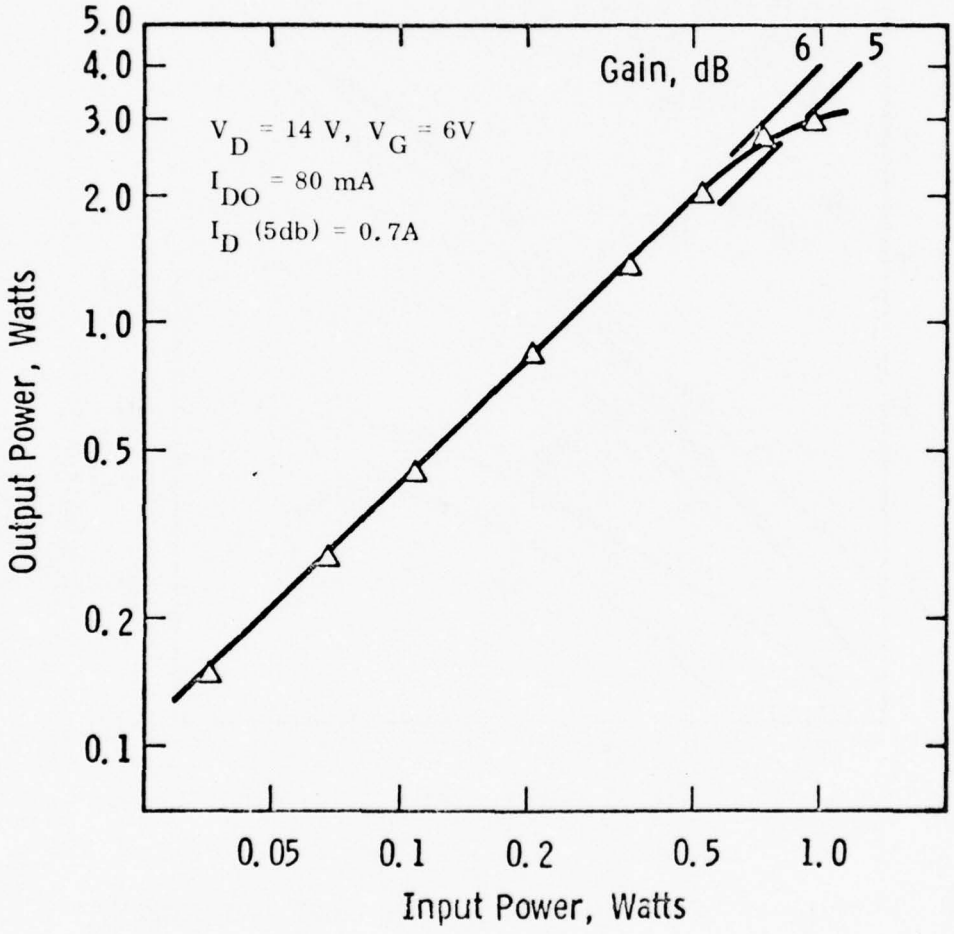


Fig. 16 — Output power vs input power for VMOST 28-3-39 at 1.0 GHz. P_{out} is 2.8W @ -1 dB compression (5.2 dB gain).

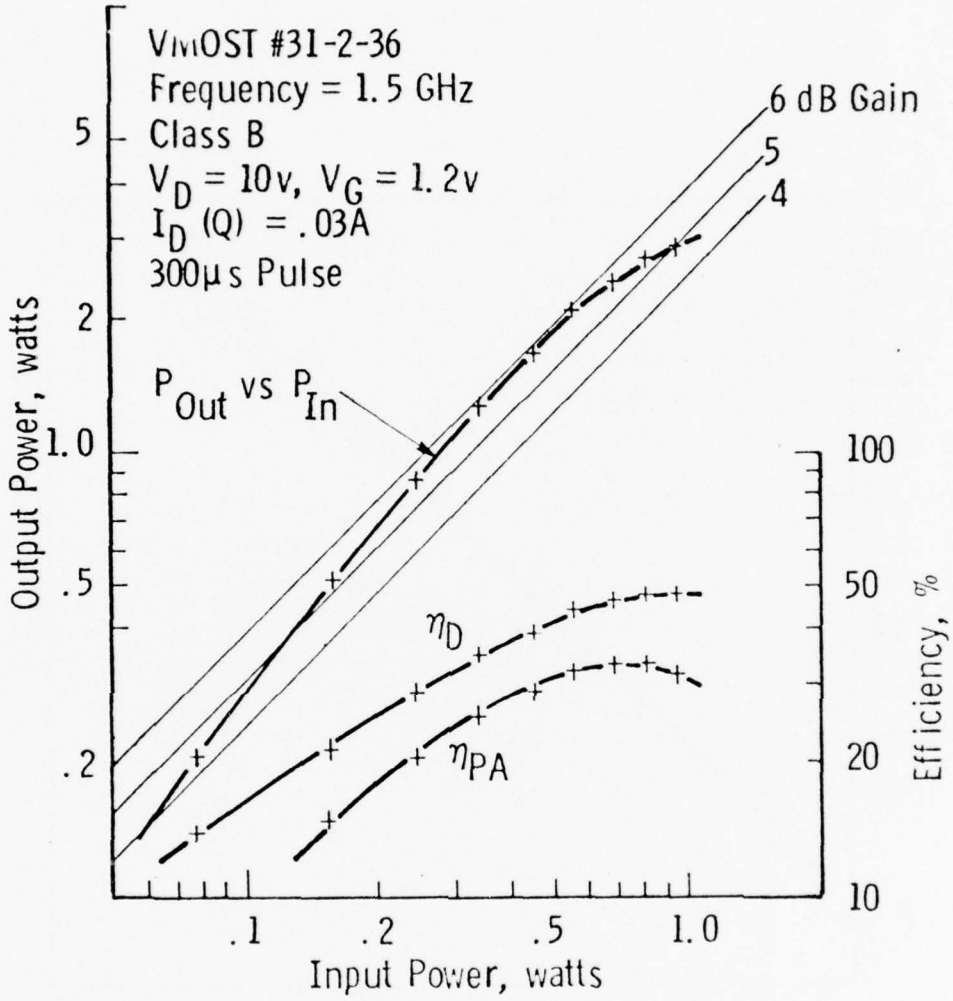


Fig. 17 — Class B Performance of 1.75 cm VMOST at 1.5 GHz

The power capability of a normal Mark V device is shown by the 1.5 GHz power curve for VMOST #33-3-8 in Fig. 18. The power at 1 dB compression is 5.5 watts with a drain efficiency of 41%. This is the highest power yet achieved by a microwave silicon MOS power transistor at this frequency. The gain of the device was unfortunately low and the device is more suitable for operation below 1.5 GHz.

The relatively constant input and output capacitances and constant transconductance of VMOST devices should result in lower distortion than in other microwave transistors. Two-tone intermodulation distortion measurements were performed on a number of Mark IV devices (operating under CW conditions) from wafer #28-3 at 1 GHz. The test signals were separated 1 MHz apart and amplified by a TWT to the required input power level. The TWT output and the VMOST output are observed on a spectrum analyzer. Figure 19 shows the third order intermodulation product (IMP) in dB below P_{out} plotted against the device output power in dBm. At the 1 dB compression point, the IMP level is 24.5 dB below the fundamental. This IMP is lower than reported values for bipolar[3] or junction-gate field-effect transistors.[4]

4.3 Discussion of VMOST Results

These power, intermodulation, and noise results are all very promising. The realization of 3 to 5W devices with a single cell unit at 1.5 GHz shows a significant improvement in both the power and frequency capability of these devices. The improvement of the frequency response of the VMOS transistors has not progressed as rapidly or as far as we had expected, however. In this section the possible and probable causes of the problem are presented together with some solutions.

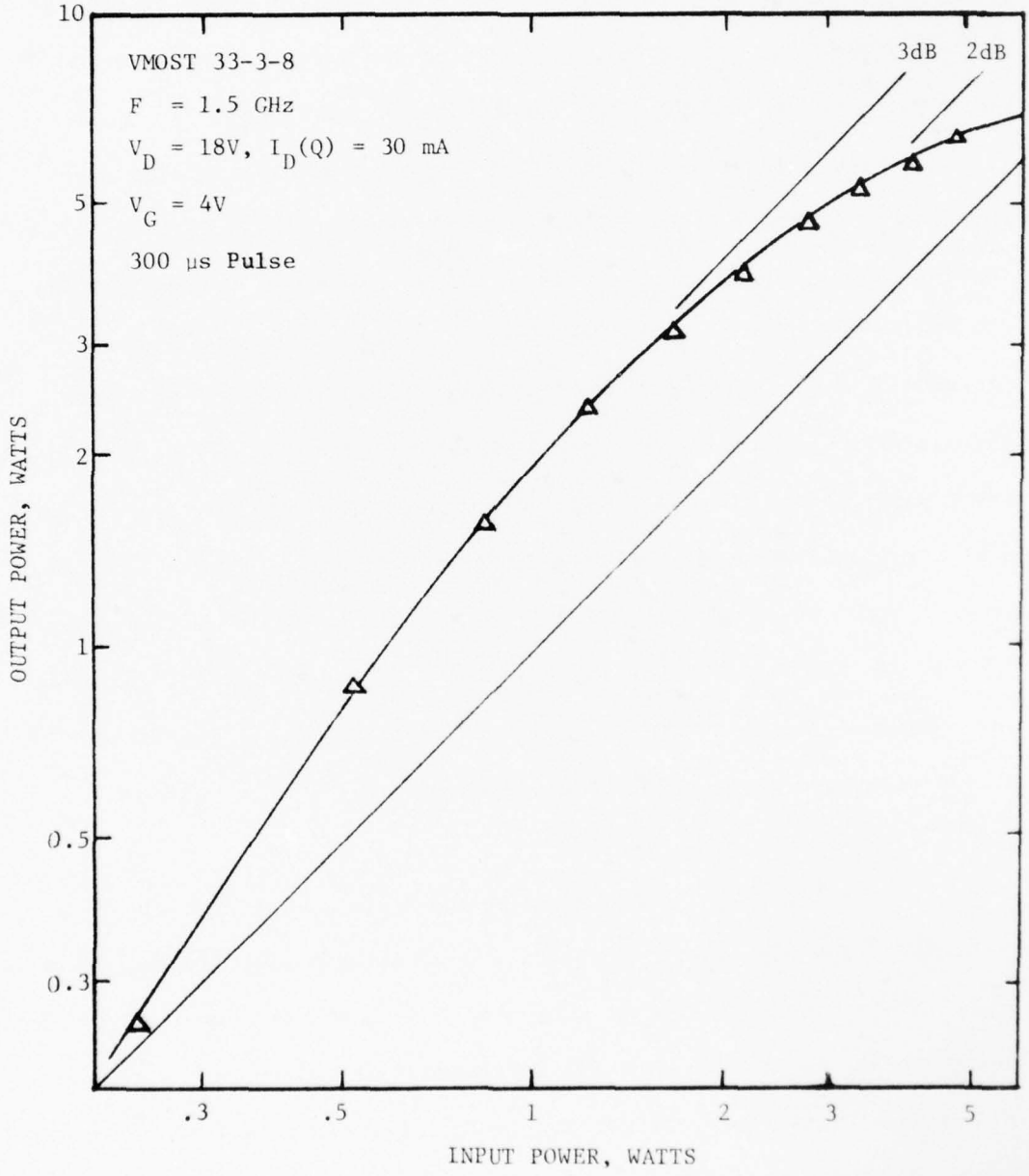


Fig. 18 — Class B Performance of Mark V VMOST

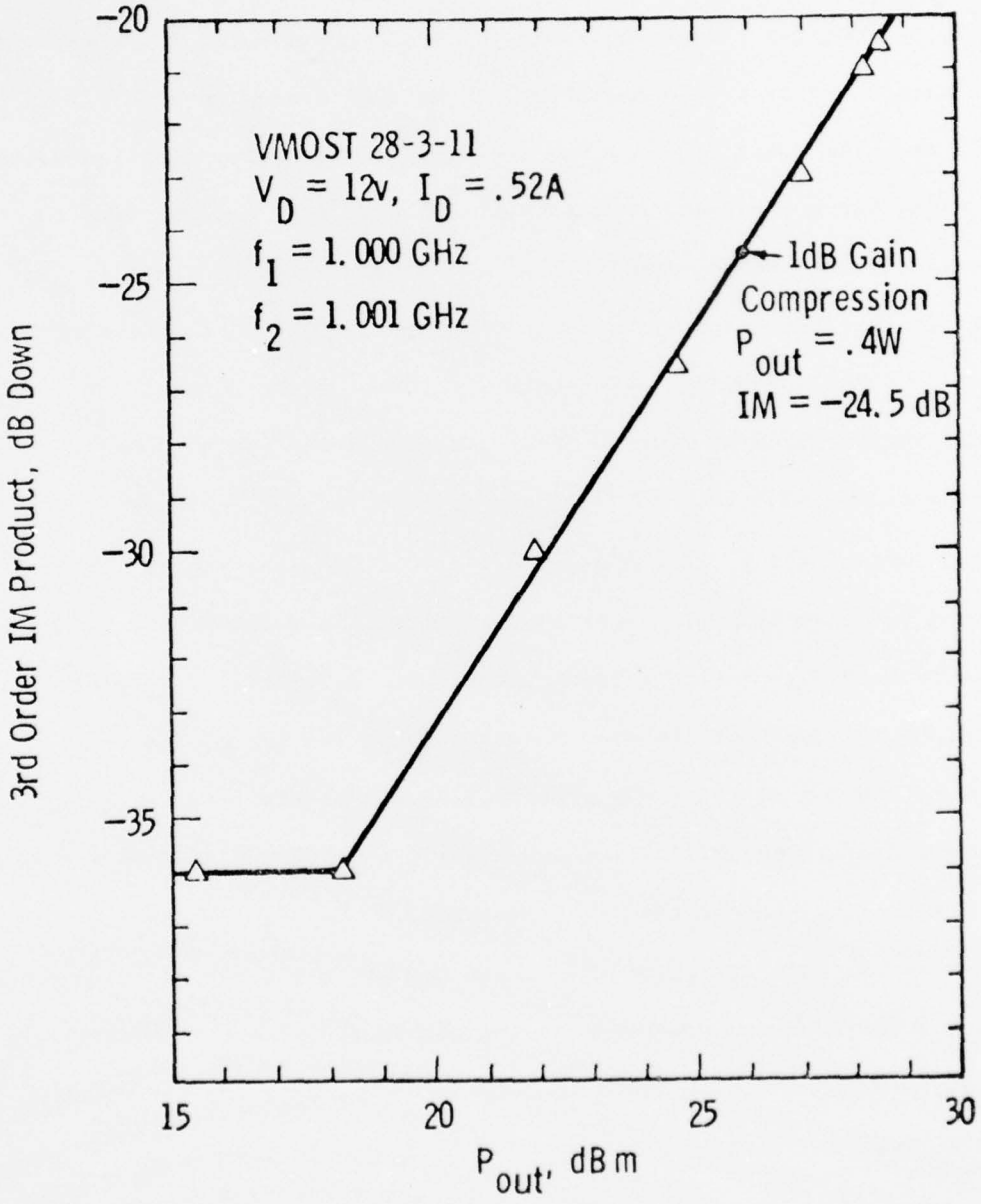


Fig. 19 — IM Product of VMOST versus Output Power

A summary of the important electrical and mechanical characteristics of seven VMOST runs is shown in Table II. All the runs are Mark V (1.72 cm) devices except Run #28-3 for which the figures in parentheses indicate the appropriate parameter values when scaled up from 1.3 cm to 1.72 cm. The first four columns show the low frequency measured values of capacitance and transconductance. The next five columns give the fabrication dimensions and the last column gives the measured f_{max} of the device. The fabrication dimensions are labeled on the drawing in Fig. 20. The column W_{n^-} represents the width of the n^- or lightly doped drain region measured from the p-n^- junction interface to where the n^- doping exceeds 2×10^{15} cm^{-3}. The notation "low n^-" indicates that the doping of the n^- region exceeds 2×10^{15} cm^{-3} and the resulting device had a poor output capacitance depletion characteristic as drain to source voltage was increased. The terms "p Depth" and "p Width" indicate the depth of the p-n^- junction below the top of the drain contact and the width of the p channel, respectively. The angle θ is the angle of the metallization evaporation and "Slit Width" is a measure of the opening between the oxide overhangs.

An examination of this chart reveals three correlations between the measured capacitances and the fabrication dimensions. The first relation concerns the output capacitance, C_{ds}, and the width of the n^- region. This is given by

$$C_{ds} \simeq \frac{\varepsilon_{Si} A}{W_{n^-}} \quad \text{for} \quad |n^-| \ll |n_A|$$

where A is the output active area of the VMOST device and W_{n^-} is the width of the n^- region. In runs #34-2 and #34-4, we see that the increase

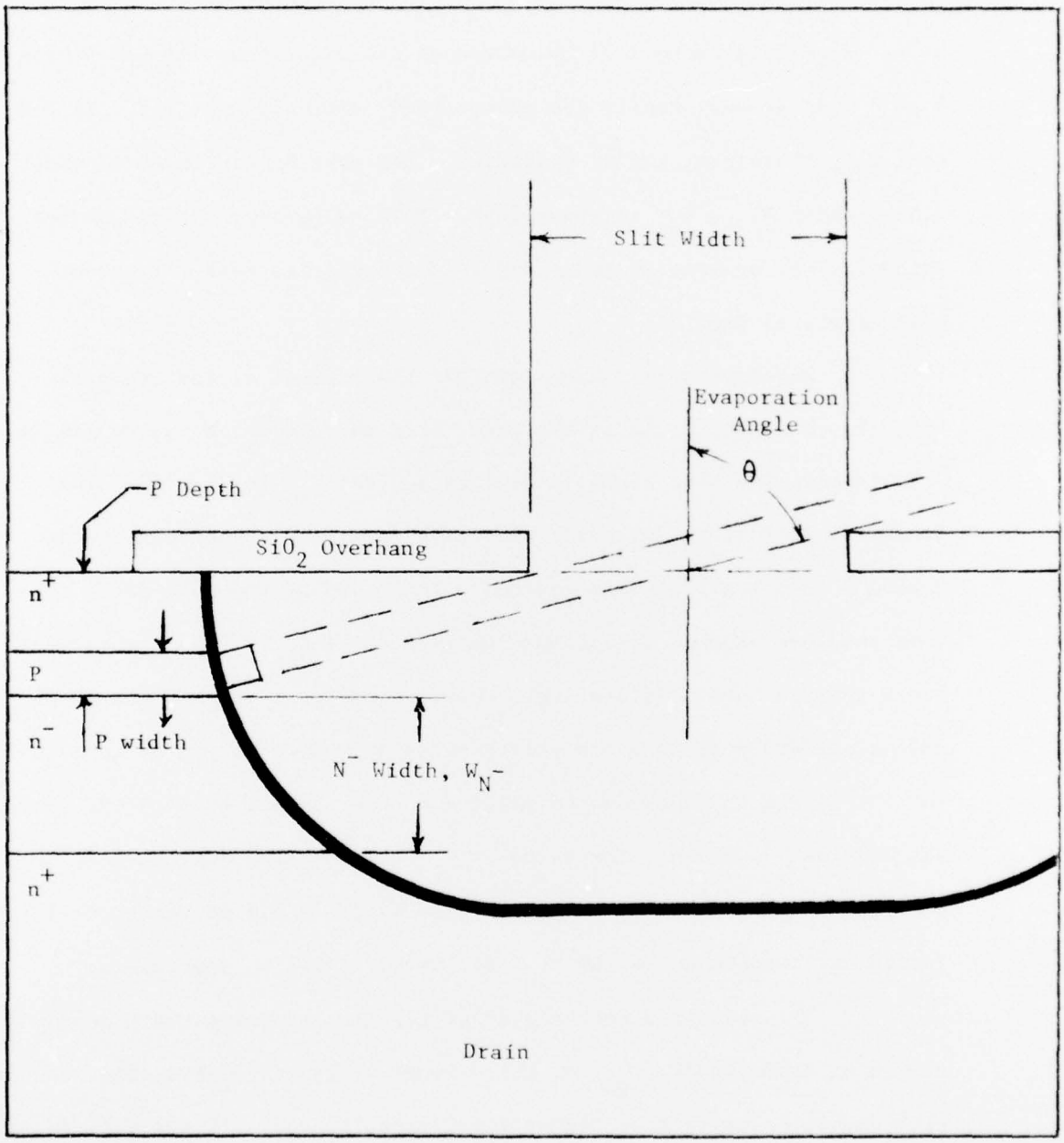


Fig. 20 — Details of Fabrication Dimensions in Table 4.1

of W_{n^-} from 1.13 μm to 1.62 μm decreases the output capacitance by about 5 pF. This is very nearly the proportional decrease expected. To control C_{ds}, therefore, the n^- epitaxial width must be increased to about 2.5 μm which drops C_{ds} to about 6 pF. This value improves the device frequency performance as indicated in the predicted Mark V frequency-gain curves of Fig. 21.

A second correlation involves the control of the feedback capacitance by the width of the oxide slit through which the device is metallized. The slit width is plotted against C_{gd} in Fig. 22. The figure shows that an emperical reduction in slit width decreases the feedback capacitance. This indicates that some of the gate metal is deposited over the n^- region and contributes to C_{gd}. Reducing the slit width thus reduces this overlap. Unfortunately, the slit width cannot be made arbitrarily small since this results in a drop in g_m, as seen in Run #32-3, due to an uncovered portion of the channel next to the source which is not inverted. The value of C_{gd} has not been a problem in most Mark V runs with narrow slit widths and a value of C_{gd} = 3.5 pF, as used in the projected performance curves of Fig. 21, is satisfied in most cases.

The third and most important relation concerns the p depth and the input capacitance, C_{gs}, of the devices. Figure 23 shows that devices with deeper p depths have higher input capacitances. If the gate metal lies over the channel alone, then the input capacitance should relate to the channel width or the slit width but not to the p depth. The explanation for the observed dependence on p depth is that the gate metal in practice is not confined to the region on the mesa side as dictated by simple

Parameter	Value
$C_{GS'}$ PF	6
$C_{GD'}$ PF	3.5
$C_{DS'}$ PF	6
C_{GN}+ PF	2
$R_{G'}$ Ω	1.1
$R_{D'}$ Ω	75
$R_{SP'}$ Ω	0.2
$R_{DP'}$ Ω	0.1
$L_{GP'}$ NH	0.2
$L_{SP'}$ NH	0.1
$G_{MO'}$ ℧	0.3

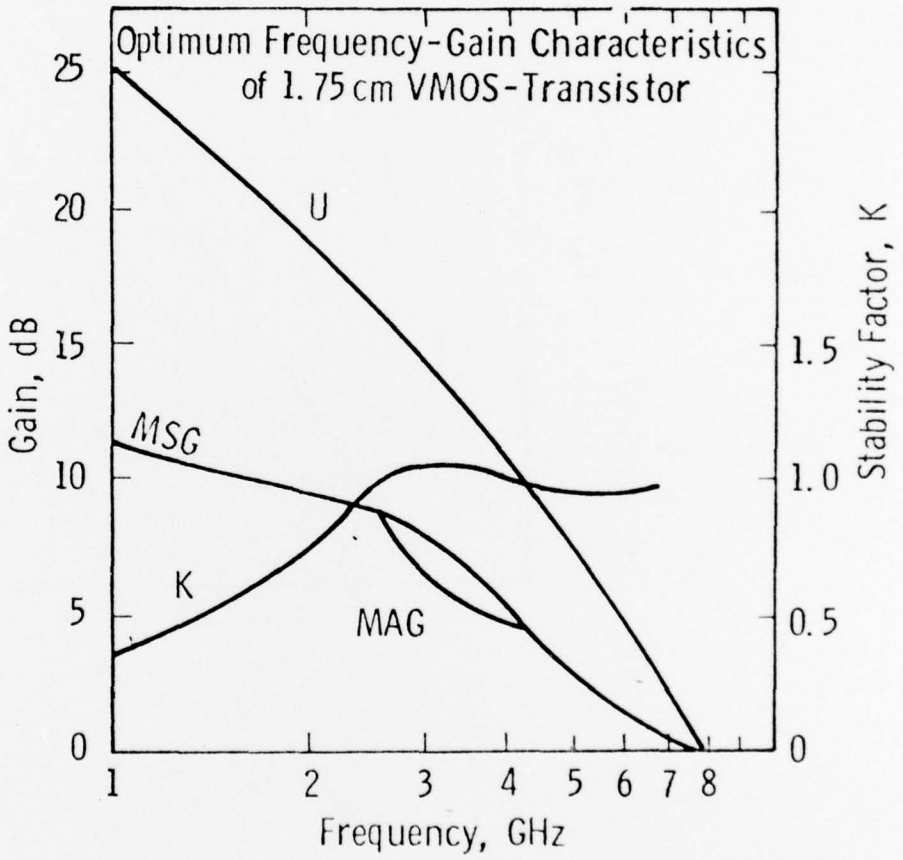


Fig. 21 — Predicted Performance of 1.75 cm VMOST

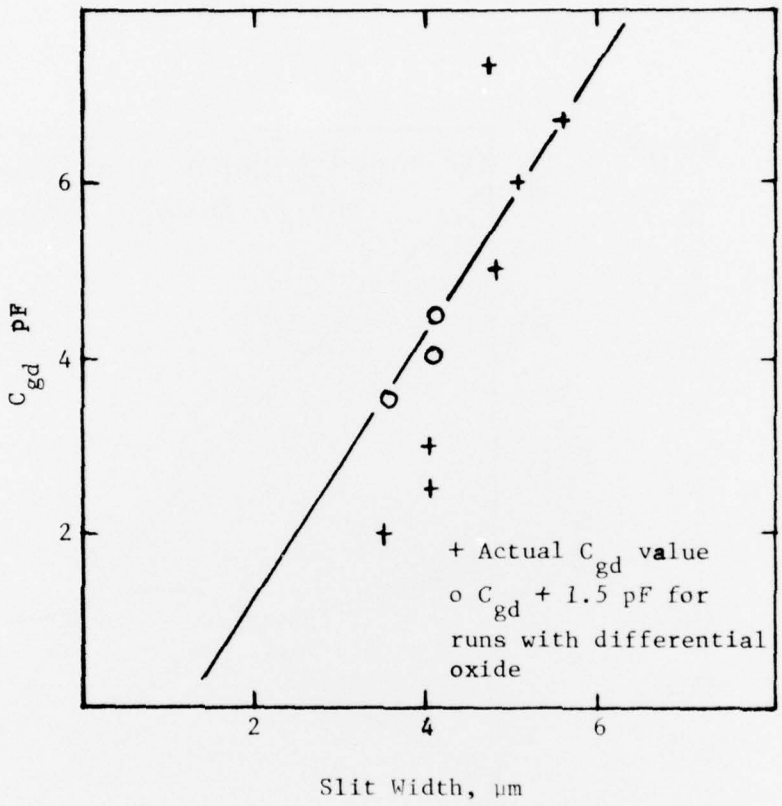


Fig. 22 - Dependence of C_{gd} on Slit Width.

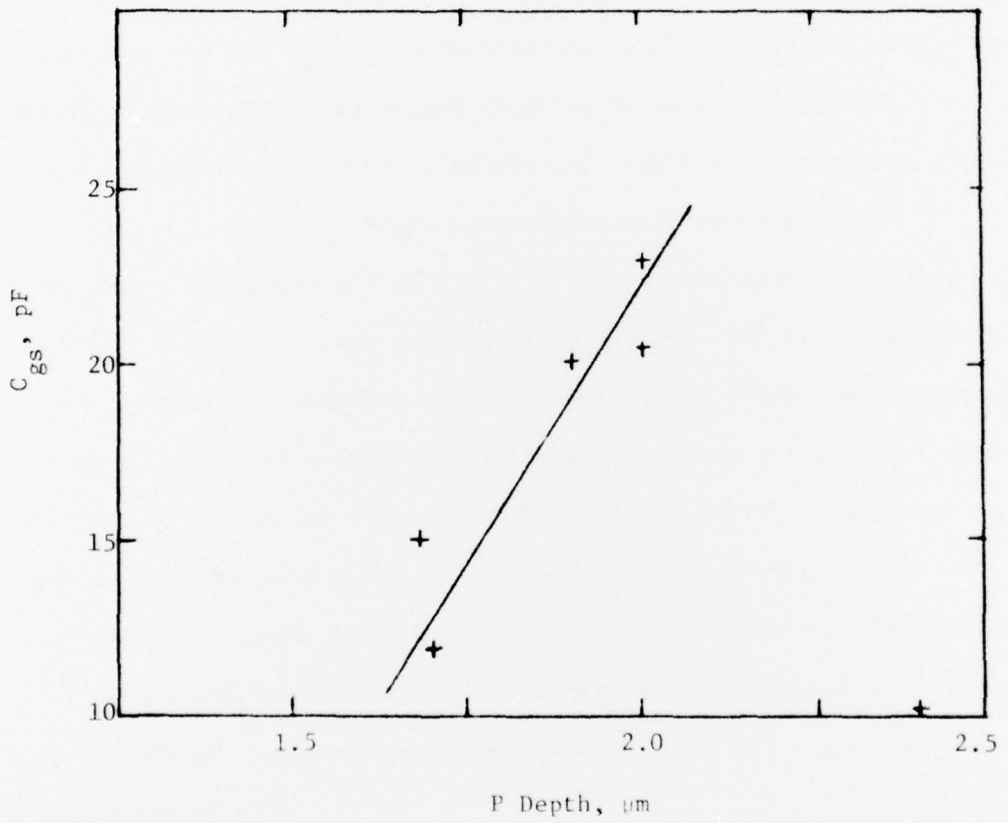


Fig. 23 - C_{gs} Dependence on P Region Depth.

geometric extrapolation, but actually coats over nearly the whole mesa side from near the top of the source down past the p-n^- junction and overlaps some of the n^- region during evaporation. Since any gate metal lying over either the source (n^+) or channel regions would contribute to input capacitance, this would relate C_{gs} to the depth of the p-n^- junction from the top of the mesa. The gate metal overlap of the n^- region has already been ascertained from the correlation of C_{gd} and slit width.

The deposition of Au at large distances within masked regions during vacuum evaporation has also recently been observed by Rossouw et al.[5] These authors have suggested a vapor-diffusion type of mechanism for the lateral transportation of Au in the evacuated region between the mask (in the case of VMOST devices, the oxide overhang) and substrate during vapor deposition onto the unshielded substrate. Subsequent condensation when supersaturation requirements are met results in Au crystallite formation well within the shielded region of the substrate. Their experimental data also rules out other possible mechanisms such as surface migration or multiple reflection between mask and substrate. The penetration distance is also a function of the angle between the evaporated metal stream and the mask plane. In VMOST devices we have found a larger penetration distance with decreased angle of evaporation.

Work is underway to reduce the diffusion mechanism by lowering the evaporation rate and decreasing the vapor concentration gradient. Preliminary results obtained in dummy VMOST type devices have shown a decrease by 30% of gate capacitance with evaporation rate reduction from 30 Å/S to 3 Å/S. This initial result is encouraging, and work is continuing to find the optimum deposition conditions for VMOST devices.

In summary, the only elements which do not meet the values required in Fig. 21 are C_{ds} and C_{gs}. C_{ds} can be reduced by growing a thicker n^- region as discussed previously, but the excess C_{gs} due to a wider gate is more fundamental and thus more difficult to solve. One possible solution is to redesign the VMOST geometry to increase the evaporation angle θ and reduce the deposition rate.

5. CONCLUSION

The work performed during this period has established that significant rf power (up to 5W) can be obtained from silicon MOS transistor devices of large gate peripheries. The usable frequency range for power operation, however, is below 2 GHz. This is a significant improvement over other MOS devices, but is still lower than the predicted frequency capability of the device.

The problems that had to be solved at the beginning of this phase of the program have almost all been solved. The one remaining problem, that of excess gate-source capacitance, is primarily responsible for the observed frequency degradation, and may be more fundamental than originally envisaged. Nevertheless, work has already begun on a redesigning of the basic VMOST geometry to reduce this parasitic.

The yield of the VMOST fabrication process is still high (> 50%) even for the large periphery 1.72 cm Mark V device.

6. RECOMMENDATIONS FOR FUTURE WORK

We recommend for future study a program to extend the intrinsic frequency of the VMOST device to 4 GHz by focussing on the following problems:

(a) Gate-Source Capacitance -- a redesign of the VMOST structure must be carried out to increase the gate evaporation angle θ.

(b) Gate-Drain Feedback Capacitance -- further reduction of gate-drain feedback can be achieved by going to an inverted (source down) geometry.

An inverted VMOST geometry which will satisfy these two requirements has been proposed and submitted for consideration (Westinghouse Proposal 5M589, August 1975).

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Silicon vertical-channel MOS-transistors (VMOST) have been designed and fabricated which exhibited high power capabilities (approaching 5 watts) at frequencies up to 1.5 GHz. Some problems with excess input parasitic capacitance still exist to limit the frequency response of the device, even though significant reductions of parasitic source and gate resistances and feedback capacitance have been achieved.

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